REMARKS

The Examiner has rejected Claims 1, 4, 5, 8, 9, 18-21, 24-27 and 30 under 35 U.S.C. 102(b) as being anticipated by Peterson et al. (U.S. Publication No. 5767856). The Examiner has further rejected Claims 2, 3, 6, 7, 10-17, 22, 23, 28, 29 under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (U.S. Publication No. 5767856) in view of Applicant's Admitted Prior Art (AAPA). Applicant respectfully disagrees with such rejections, especially in view of the amendments made to the independent claims.

With respect to such amended independent claims, the Examiner has relied on Figure 2 and the following excerpt from Peterson to make a prior art showing of applicant's claimed "sending an instruction request to video memory utilizing a texture module" (see this or similar, but not identical, language in each of the foregoing claims).

> "The information in the attribute queue is extracted in a first-in-first-out basis to continue down the pixel pipeline for processing by the functional units of the pixel engine. As discussed above, at the time read requests were made, instructions were placed in the attribute queue as to how to extract data from read data queue 245. As these instructions are encountered when processing the contents of the attribute queue, control logic 265 extracts information from the read data queue to send down the pixel pipeline..." (Col. 4, lines 59-67)

The Examiner has relied on Peterson's "attribute queue" (see excerpt above and Fig. 2, item 220) to meet applicant's claimed "video memory." However, the attribute queue 220 is a component of the only entity in the Peterson reference that could be considered a texture module, as claimed by applicant. Thus, under the Examiner's logic, if the attribute queue 220 in Peterson were to be the same as applicant's claimed "video memory," then, to meet applicant's claims, the texture module that sends the instruction request to the video memory would have to send the instruction request to itself. Since this is illogical, the Peterson reference clearly cannot meet applicant's claimed "sending an instruction request to video memory utilizing a texture module" (emphasis added).

Likewise, the Examiner's rejection of applicant's claimed "receiving instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline" is also deficient. Again, if the attribute queue 220 is to be considered the video memory, as the Examiner suggests, then the texture module would be sending the instruction request to, and receiving the instruction request from, itself.

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. Verdegaal Bros. v. Union Oil Co. Of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. Richardson v. Suzuki Motor Co.868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

This criterion has simply not been met by the Peterson reference, as noted above. Nevertheless, despite the foregoing paramount distinctions and in the spirit of expediting the prosecution of the present application, applicant has clarified each of the independent claims to further distinguish the prior art of record.

In particular, applicant has amended nearly all of the independent claims to further clarify that it is the texture module that sends the request to the video memory. Specifically, the claims have been amended as follows:

> "sending an instruction request to video memory ~~utilizing~~, where a texture module in a graphics pipeline sends the instruction request to the video memory; and
>
> receiving instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline" (see this or similar, but not identical, language in each of the foregoing claims).

A notice of allowance or a specific prior art showing of all of applicant's claim limitations, in combination with the remaining claim elements, is respectfully requested.

Applicant further notes that the prior art is also deficient with respect to the dependent claims. For example, with respect to dependent Claims 4 and 5, the Examiner has relied on the following excerpt and Figure 1 of Peterson respectively, to make a prior art showing of applicant's claimed "wherein the video memory includes a frame buffer" (Claim 4) and "wherein the video memory includes direct random access memory (DRAM)" (Claim 5).

> "A data flow diagram for the output end of the pixel engine pipeline is illustrated in FIG. 3. The output of the pixel engine will eventually be sent to system memory or the video buggers (154 in FIG. 1)." (Col. 5, lines 3-7)

Applicant respectfully asserts that the above excerpt and Figure 1 from Peterson teach that the output from the pixel engine is sent to memory. However, the "video memory" in applicant's foregoing claims relates to where the instruction request is sent, and not simply to where output of an entire pixel engine is sent. Furthermore, the instructions in Peterson are only sent to the attribute queue (see Col. 3, lines 63-66), and thus are NOT sent to a frame buffer or DRAM, in the manner claimed by applicant.

With respect to dependent Claims 18-19, the Examiner has simply relied on Figure 2 of Peterson to make a prior art showing of applicant's claimed "wherein a complete instruction set is received in response to the instruction request" (Claim 18) and "wherein a partial instruction set is received in response to the instruction request" (Claim 19).

Applicant respectfully asserts that nowhere in Figure 2 is there any disclosure of an "instruction set," either complete or partial, as claimed by applicant. All Peterson discloses with respect to instructions is that commands are sent from the command queue to the attribute queue, where "[t]he commands include

instructions as to how many bytes should be retrieved from the read data queue 245" (see Col. 3, lines 63-66). Thus, there is clearly no disclosure of receiving "instruction sets," in the manner claimed by applicant.

Again, the aforementioned anticipation criterion has simply not been met by the Examiner's reference. A specific prior art showing of such claim limitations or a notice of allowance is respectfully requested. All of the pending independent claims are thus deemed allowable along with any claims depending therefrom.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. For payment of any fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP064/P000286).

Respectfully submitted,

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